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TITLE: Bus keeper circuit

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PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE
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KR 2002061893 A	July 25, 2002	N/A
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ABSTRACTED-PUB-NO: KR2002061893A

BASIC-ABSTRACT:

NOVELTY - A bus keeper circuit is provided to easily embody a circuit designed as a three-state bus structure to an FPGA(Field Programmable Gate Array) and to make the circuit carry out a stable operation by applying to the FPGA.

DETAILED DESCRIPTION - A NAND gate(46) generates a high level signal if one of the enable signals(EN1-EN6) is the low level. A three-state driver(44) makes the output signal of a flip-flop(42) feedback to the three-state bus and an input terminal(D) of the flip-flop(40) by responding to the output signal of the NAND gate of the low level. The flip-flop(42) stores the data

output from the three-state driver by responding to a clock signal(CLK). In this case, the bus keeper circuit keeps the previous data stored in the flip-flop(42) because the data, transferred to the three-state bus from the function blocks, do not exist. The bus keeper circuit makes the flip-flop stores the data transferred to the three-state bus by responding to the clock signal and in case of not existing the data transferred to the three-state bus, transfers the data previously stored data output from the flip-flop by making the three-state driver enabled.

CHOSEN-DRAWING: Dwg.1/10

TITLE-TERMS: BUS KEEPER CIRCUIT

DERWENT-CLASS: T01

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